Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Dissemination kit

Deliverable no.: D7.7
Due date: 31/7/2015
Actual Submission date: 31/7/2015
Authors: AIT, UVEG, KIT, IMEC, UGent, TU/e
Work package(s): WP7
Distribution level: PU[1]
Nature: document, available online

List of Partners concerned

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PP = Restricted to other programme participants (including the Commission Services)
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Summary

In this dissemination kit we present the most important achievements of the NAVOLCHI project for plasmonic interconnects for chip-to-chip communication. Specifically, it presents the most important results for the several components that have been develop in NAVOLCHI; the plasmonic modulator, the plasmonic pre-amplifier, and the plasmonic photodetectors. It also presents the most important figure with a detailed description for each figure.

1. Contents

1. The NAVOLCHI project

In order to fulfill the demand for ever higher data processing capability, next generation processors will be realized with multi-core systems. Multicore systems have been identified as the most promising, scalable and power efficient method for integrating larger number of CMOS circuits. The transition to many-core microprocessor architectures is expected to drive increased chip-to-chip I/O bandwidth demands in processor, processor-memory interfaces and in multi-processor systems in the range of 200 Gbit/s to 1 Tbit/s. To this point electrical interconnects are used. However, this technology not only suffers from limited bandwidths but also from electrical cross-talk, frequency-dependent loss (dispersion), and high power dissipation. Current photonic technologies, which are optimized for long distance telecommunication and data communication applications, do not meet the necessary metrics (footprint, power dissipation, form factor, cost, and signal integrity) needed for interconnects between high-speed electronic chips. Ideally, future generations of super high computing systems will rely on optical interconnects offering several terahertz bandwidths at low loss for on chip-to-chip and board-to-board communications with better crosstalk-noise immunity.

These obstacles can be overcome exploiting Surface Plasmon Polaritons (SPP). SPPs are electromagnetic surface waves coherently coupled to charge density oscillations bound to a metal-dielectric interface. Due to the combined electronic and photonic nature, these waves can be confined well below the usual diffraction limit imposed by wave mechanics. Along with the confinement comes an enhancement of the electromagnetic field, allowing for an increased strength of light-matter interaction, in particular of nonlinear interactions. Optical devices that exploit the unique properties of SPPs have the potential to overcome the limitations in bandwidth of nowadays state-of-the-art interconnects, either electrical or optical. This is a consequence of the ultra-fast electronic interaction times, as well as the short carrier transit times through the sub-micron device cross sections. At the same time, the small footprint of the order of a few square microns promises a high integration density on-chip, such that a plasmonic interconnect solution may outperform all other conventional solutions.

NAVOLCHI objectives

The NAVOLCHI project explores, develops and demonstrates a novel nano-scale plasmonic chip-to-chip and system-in-package interconnection platform to overcome the bandwidth, footprint and power consumption limitations of today’s electrical and optical interconnect solutions. The technology exploits the ultra-compact dimensions and fast electronic interaction times offered by SPPs to build plasmonic transceivers with a few square-micron footprints and speeds only limited by the RC constants. Key elements developed in this project are monolithically integrated plasmonic lasers, modulators, amplifiers and detectors on a CMOS platform. The transceivers will be interconnected by free space and fiber connect schemes. The plasmonic transceiver concept aims at overcoming the challenges posed by the need for massive parallel inter-chip communications. Yet, it is more fundamental as the availability of cheap miniaturized transmitters and detectors on a single chip will enable new applications in sensing, biomedical testing and many other fields where masses of lasers and detectors are needed to e.g. analyze samples. Economically, the suggested technology is a viable approach for a massive monolithic integration of optoelectronic functions on silicon substrates as it relies to the most part on the standardized processes offered by the silicon industry. In addition, the design and production cost of plasmonic devices are extremely low and with their dimensions 100 times smaller over conventional devices they will require much lower energy to transfer data over short ranges of multi-processor cluster systems. This project has the potential to create novel high-impact technologies by taking advantage of the manifold possibilities offered by plasmonic effects.

The Si-plasmonic technologies implemented by NAVOLCHI rely on the ultra-compact and high-performance plasmonic components that have been developed in the framework of the project:

On the transmitter side of the interconnect system, ultra-compact lasers and modulators transfer electrical signals to the optical domain. The transmitter chip consists of an electrically pumped hybrid plasmonic indium phosphide (InP) laser on a silicon waveguide structure and a plasmonic Si based modulator to externally encode data at the rate of up to 100 Gbit/s. The small footprints of both plasmonic laser as well as modulator make their combination perfect for realization of an optical transmitter chip with dimensions comparable to electronic devices. Thus, it is possible to build several tens to hundreds such Si based transmitter modules integrated together using standard high-volume, low-cost silicon CMOS manufacturing technologies in order to produce low-cost, ultra-small size photonic chips. This kind of plasmonic compact transmitter chip can be a solution for high speed, low cost interconnection between various electrical chips. In addition the breakthrough dimensions of the plasmonic laser and modulator create a possibility to efficiently combine clusters of plasmonic transmitters on the same chip. Replacing the electrical interconnects from current electrical chips with high speed plasmonic interconnects becomes possible without significantly increasing the footprint of the electrical chip.

The main objectives for the transmitter consist of

- Fabricate electrically pumped plasmonic/metallic nano-laser devices bonded onto an SOI wafer with light coupled into either a plasmonic or conventional SOI waveguide.
- Performance targets for the laser are an active region area less than approximately one square micron, and optical output power coupled into the waveguide of at least approximately 100 microwatts with an attempt to achieve output powers up to one milliwatt.
- Plasmonic modulators with more than 3 dB extinction ratio and device lengths below 10 µm will be demonstrated.
- Modulation speeds up to 40 Gbit/s are demonstrated.

The objective to develop a receiver for chip-to-chip interconnection is to measure light under low input power level conditions. Such a receiver will potentially comprise a plasmonic optical amplifier in order to deliver appropriate signal level to the on-chip detector and a photodetector for a signal at the specific wavelength with a footprint comparable to the other devices developed on the chip. Amplifier and detector can make use of colloidal quantum dots eventually embedded into conductive polymers to define micrometric photodetectors on Si substrates or directly into nano-gaps between metal nano-contacts.

The main objectives for the receivers are:

- Electrical injection of quantum dot based plasmonic amplifier
- 10dB on-chip gain for quantum dot based plasmonic amplifier
- Quantum efficiencies above 80 %
- Responsivities above 0.1 A/W

Further objectives deals with the realization of the key optical passive components such as optical gratings, optical filters and plasmonic couplers to be employed in plasmonic transmitter and receivers for on-chip coupling between single components and inter-chip coupling. Both, for the optical modulator and the optical amplifier we need to couple light efficiently from a standard silicon waveguide –which is used for transporting the signals over the chip -to a highly confined plasmonic waveguide –which is used for realizing ultra-compact and efficient active devices. In particular NAVOLCHI demonstrates metallic taper and directional couplers for light coupling from silicon nanowire into the plasmonic MIM waveguides used for realizing the modulator with a coupling efficiency exceeding 35%.

2. Plasmonic Transmitter

2.1. *Plasmonic laser*

NAVOLCHI has developed a waveguide-coupled laser with a metallic nano-cavity. We performed the design of a plasmonic and a metallo-dielectric laser, both coupled to an InP waveguide. We carried out the fabrication of the metallo-dielectric version in a III-V membrane on silicon as shown in Figure 1.

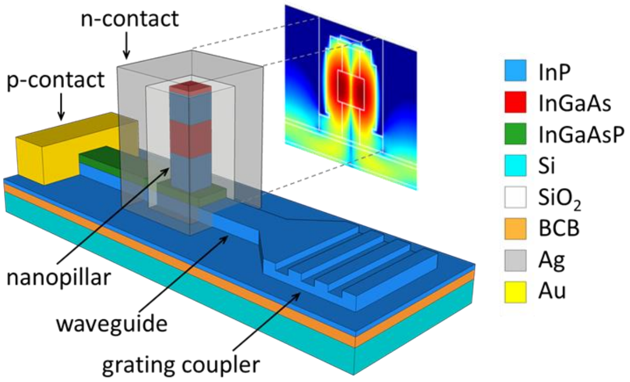

Figure 1: (a) Schematic representation of the nanopillar laser device coupled to an InP-waveguide, on a silicon substrate. The layer stack from top to bottom is: InGaAs(100nm) /InP(350nm) /InGaAs(350nm) /InP(600nm) /InGaAsP(200nm) /InP(250nm) /BCB /Si. The inset shows the spatial profile of the modulus square of the electric field of the main cavity mode in logarithmic scale to visualize the waveguide coupling.

Modelling of Si-plasmonic modulators

Within the framework of NAVOLCHI, two different modulator approaches have been studied; direct amplitude modulation employing surface plasmon polariton absorption modulator and phase modulation with plasmonic phase modulator.

Fabrication of plasmonic/metallic laser

Figure 2 shows SEM (Scanning Electron Microscope) of the fabricated devices. Although lasing behavior was not observed, we demonstrated the first metal-cavity light emitting diode (LED) coupled to a waveguide on silicon. The device showed relatively high external quantum efficiency (ranging from 10^{-4} to 10^{-2} at room-temperature and 9.5 K, respectively) compared to state-of-the-art nanoLEDs with efficiencies in the 10^{-7} to 10^{-5} range. Additionally, the device showed sub-nanosecond electro-optical response as discussed below.

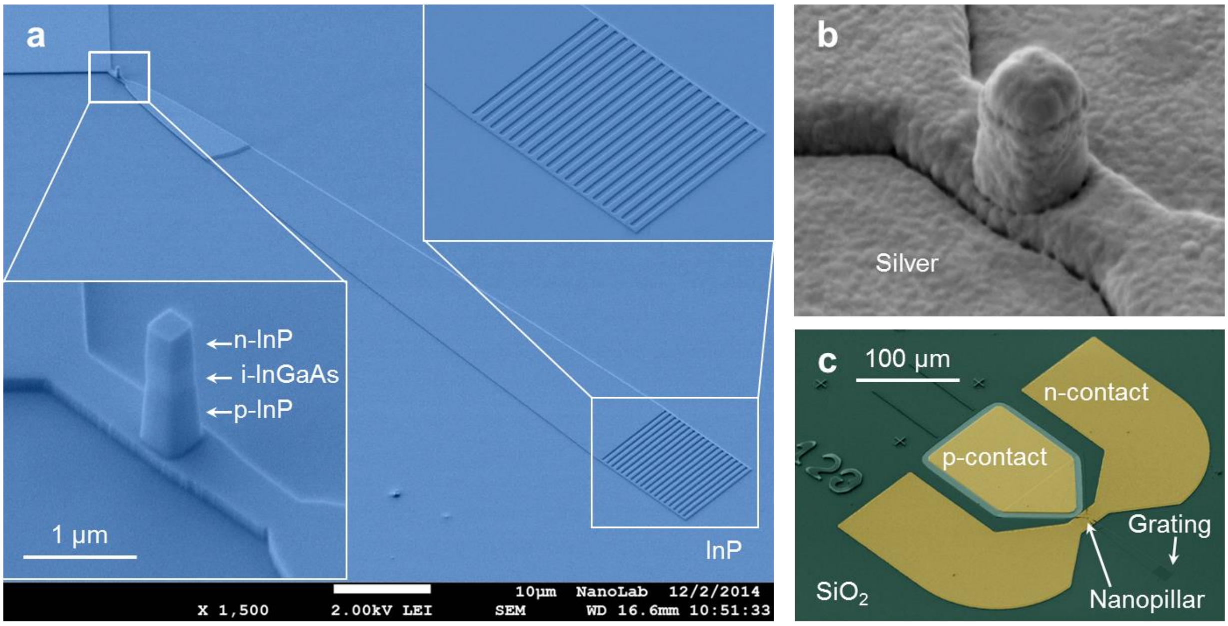

Figure 2: (a) SEM image showing the fabricated device structure before metallization. The nanopillar lies on top of a waveguide connected to a grating coupler. (b) Metal-coated nanopillar after silver evaporation and annealing. (c) Panoramic view of the device after metallization to fabricate the electrical p- and n-contacts.

2.2.Plasmonic modulator

Within NAVOLHCI, we realized our plasmonic modulators based on a silicon-on-insulator wafer having a 2 µm thick buried oxide and a silicon device layer with a thickness of 220 nm. Silicon nanowire waveguides with a width of 450 nm and a height of 220 nm are used as access waveguides to the phase modulator sections. Light is coupled in and out of the silicon nanowires using silicon grating couplers. The binary phase shift keying (BPSK) modulator is constructed of a single high-speed plasmonic phase shifter (PS) with a length of L = 29 µm operating as a phase modulator (PM). Figure 3(a) gives an artist’s impression of the POH PM. Mode conversion between the quasi–TE mode of the silicon waveguide and the gap surface plasmon polariton (SPP) is accomplished via a tapered silicon waveguide enclosed by a tapered gap plasmon waveguide. The phase of the optical signal is modulated in the 29 µm long plasmonic PM section. High-speed phase modulation is performed by the PS exploiting the Pockels effect in an electro-optic organic cladding material. Applying a voltage between the metal electrodes changes the refractive index of the electro-optic (EO) material in the slot due to the Pockels effect, and therefore influences the phase velocity of the plasmonic mode. The silicon photonic-layer-circuit (PLC) is fabricated using standard processes such as 193 nm DUV lithography and Si dry etching in the framework of ePIXfab. The metallic slots having widths of ~150 nm are defined on the silicon PLC with electron-beam lithography and a lift-off process with poly-methyl-methacrylate (PMMA) resist.

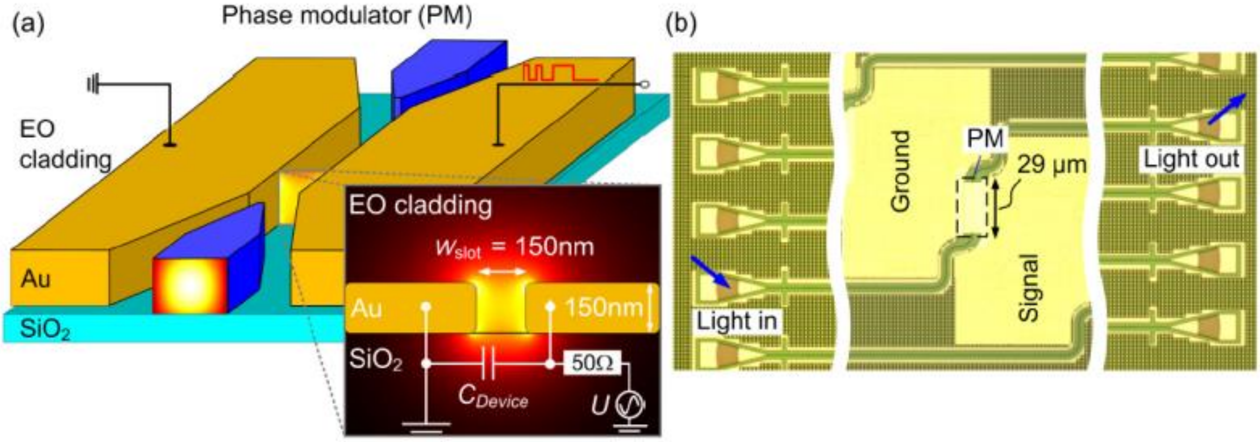

Figure 3: Plasmonic-organic hybrid (POH) phase modulator (PM) fabricated on the silicon-on-insulator (SOI) platform. (a) Schematic of the POH PM comprising a metallic slot waveguide filled and clad with an electro-optic (EO) material. The photonic mode of a silicon nanowire waveguide (blue) is converted to a gap surface plasmon polariton (SPP) via a tapered silicon waveguide enclosed by a tapered gap plasmon waveguide. The inset shows a cross section of the device with the mode field of the SPP in the gap. In addition, a lumped-element equivalent circuit of the PM is given. The device can be represented by a capacitor (C_{Device} ≈1.5…3 fF, length dependent). (b) Optical microscope photograph of the fabricated POH PM. Light is launched in and out of the silicon waveguide via diffraction grating couplers. The phase of the optical signal is modulated in the plasmonic modulator section having a length of 29 µm.

Mach-Zehnder modulator

For the MZM, two high-speed PS with a common signal electrode are fabricated in ground-signal-ground configuration as depicted in Figure 4(a) and (b). In the case of the POH MZM, we employ the EO material SEO100 (Soluxra, LLC) because of its excellent thermal stability up to 85°C, which is an important requirement for use in real-word communication systems. The electro-optic effect in the EO materials is activated through a poling procedure. The static characterization of the MZM can be retrieved in [11].

We perform data modulation experiments with our POH MZM using a direct receiver setup. An electrical non-return-to-zero (NRZ) signal with PRBS pattern length of 2^{31}-1 and with a peak-to-peak voltage swing of 5 V (measured across a 50 Ω resistor) is fed to the modulator via a ground-signal-ground (GSG) RF probe. The operating point for the MZM is defined by selecting the operating wavelength. The MZMs are operated in the quadrature points, i.e., the modulator output intensity changes linearly with the relative phase difference of the two arms. The OOK signal after the MZM is detected with a standard pre-amplified direct receiver comprising a single EDFA, an optical band-pass filter with a bandwidth of 2 nm, a bit-error-ratio tester (BERT), and a digital communication analyzer (DCA).The eye diagrams measured after the MZM with 29 µm long PS sections for bit rates of 30 Gbit/s (BER = 2×10^{-5}), 35 Gbit/s (BER = 3×10^{-5}) and 40 Gbit/s (BER = 6×10^{-4}) shows that these BER are well below the threshold of 4.5×10^{-3} for hard-decision FEC codes with 7% overhead.

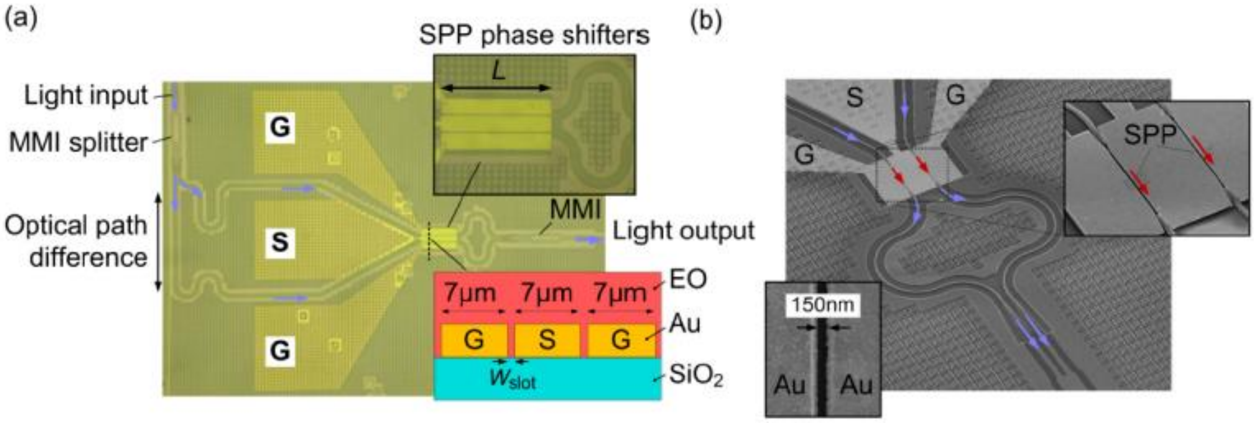

Figure 4: Plasmonic-organic hybrid (POH) Mach-Zehnder modulator (MZM), fabricated on the silicon-on-insulator (SOI) platform. (a) Optical microscope image of the fabricated MZM. The Mach-Zehnder interferometer (MZI) is fabricated on the silicon-on-insulator (SOI) platform using low-loss photonic MMI couplers for light splitting and combing. An optical path difference is implemented in the MZI, and the operating point is selected by choosing the operating wavelength. For modulation, an optical phase difference between the two arms is induced by the SPP phase shifters [19]. (d) Scanning electron microscope (SEM) picture of the silicon-plasmonic MZM. The modes of the silicon waveguide are coupled to the plasmonic phase PM sections, which modulate the phase of the SPPs.

3. Plasmonic Receiver

3.1.Polymer-QD Based Plasmonic Amplifiers

UVEG concentrated their efforts toward the designs using polymer-QD layers on top of metallic linear waveguides have been successfully fabricated and characterized using a novel technique for probing the SPP propagation. The active material proposed in this architecture consisted of a nanocomposite composed by the dispersion of semiconductor nanocrystals or colloidal quantum dots (QD) in polymers (PMMA mainly) or bilayers formed by PMMA and close-placked QD layers. Linear plasmonic waveguides were patterned by ebeam lithography on Si-SiO_2 substrates and defined by the lift-off of an evaporated Au film around 25 nm thick. They were characterized by using a novel method to measure the propagation length of the SPP propagating in those metal waveguides. In a second step we will study the possible enhancement of the L_p when the QD-polymer nanocomposite (or bilayer) forming a dielectric planar waveguide is optically pumped by end-fire coupling, as illustrated in Figure 5(a). Even if polymer-QD layers do not exhibit amplification of the spontaneous emission (ASE), a noticeable compensation of the SPP propagation length was demonstrated at visible wavelength, from around 60 mm without pumping up to more than 1 mm under 11 mW laser pumping, as shown in Figure 5(b) for a linear Au-waveguide 250 nm wide.

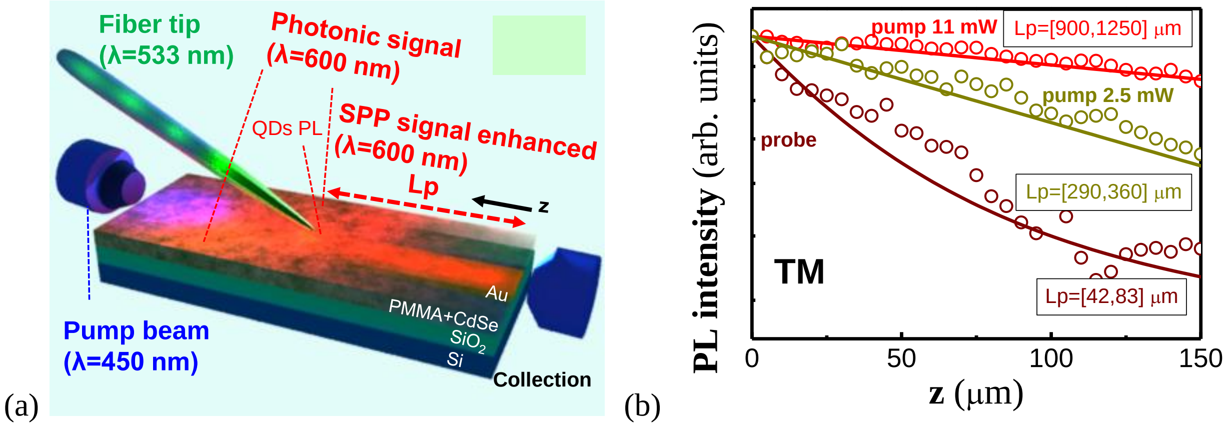

Figure 5: (a) SPP excitation with a fiber tip; the tip provides a small spot on the PMMA-QD film at a wavelength of 533 nm; the QD PL is coupled to the waveguide modes (LR-SPP mainly); the loss compensation is achieved by coupling a pump beam (450 nm) at the opposite edge of the waveguide where the SPP is being probed. (b) PL intensity as a function of the distance between the tip and the edge of the sample in TM measured in a 250 nm wide Au waveguide without (wine) and under two pumping conditions (dark yellow and red); clearly the propagation length, Lp, increases with the power of the pumping beam; symbols correspond to the experimental data and the curves lines to a exponential decay fitting.

3.2.Patents Plasmonic QD based photodetectors

Along the project UVEG have optimized the synthesis of PbS QDs with absorption/emission at wavelengths around 1550 nm, as also the deposition (+ ligand exchange) of thin films in the thickness range 300-500 nm by means of a Dr.Blading technique. These QD-solid films exhibit a reasonable uniformity (Figure 6(a)) and have a typical resistivity around 10^5 ucm, a hole concentration larger than 10^{15} cm^{-3} and mobilities smaller than 0.065 cm^2/Vs, as estimated from Hall measurements.

Schottky-heterostructure photodiodes

In the case of the most outstanding generation of Schottky-hererostructure devices the UVEG team has obtained peak responsivities of 0.48 and 0.18 A/W at around 1300 and 1500 nm (blue and green lines in Figure 6(b)). The time response of these photodiodes working in photocurrent mode is limited to be around 100 us, very similar to values reported in literature. The photovoltage noise was measured to be of the order of 85 nV/Hz$^{1/2}$ at 1 kHz for the photodiode based in the 500 nm thick PbS QD film, whereas the photocurrent was perfectly linear over more than three orders of magnitude (constant responsivity). The experimental detectivity was estimated in the range 10^{12} - 10^{13} Jones. Finally, it is also worth noting that fabricated photodiodes (without encapsulation) are stable in air during several weeks, even if electrical parameters degrade progressively (after one month in air the responsivity decreased a factor two), possibly due to the protecting effect of the top metal electrode (Ag).

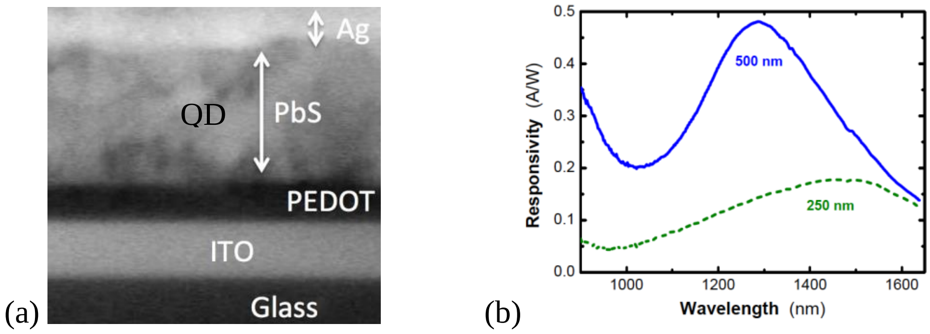

Figure 6: (a) Transversal SEM image of a complete Schottky photodiode. (b) Responsivity measured in the best fabricated photodiodes using the same PbS QDs to deposit 250 (green dashed line) and 500 nm (blue continuous line) thick films.

2. Optical and Electrical Interfaces

NAVOLCHI also focused on realizing the optical and electrical interfaces for the plasmonic interconnection platform. KTH developed optimised couplers between silicon and plasmonic waveguides. Through process and design improvements the losses for this coupling are now below 1dB. In parallel also the simulation of a novel side coupler was carried out. IMEC demonstrated different types of optical filters and developed several types of novel grating couplers. ST developed the interfaces between the electronic drivers and the optical devices.

Modelling and fabrication of coupling Si waveguide to plasmonic waveguide

Tapered Couplers: The tapered couplers for coupling light into the plasmonic modulators were numerically optimized, fabricated and tested. Several generations have been realized. The mode converters have been fabricated as a part of plasmonic modulators. The modulators with various device lengths and with a slot size of 140 nm and 200 nm were fabricated on a silicon on insulator (SOI) platform, where the silicon nanowire waveguides are used as access waveguides. Optical and scanning electron microscope images of the first generation device with device length of 34 μm and the slot size of 200 nm are given in Figure 7(a) and (b), respectively.

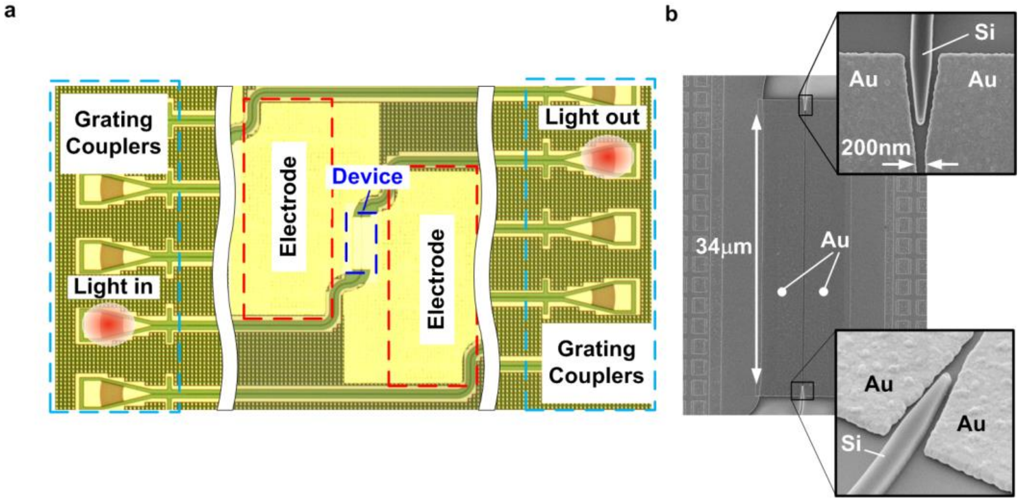

Figure 7: Fabricated plasmonic phase modulator on silicon on insulator platform. (a) Optical microscope image of the device. Silicon nanowire waveguides are used as access waveguides for the plasmonic modulator. Light is launched in and out from the chip using grating couplers. (b) Scanning electron microscope image of the modulator with a length of 34 m and a slot size of 200 nm. Metallic tapers are used for photonic to plasmonic mode conversion.

Integrationin fully working interconnects

The **Dual Die Communication Module** (abbreviated **DDCM**) is the building-block responsible for the interconnection of different dice within a so called Network in Package (NiP), the communication system enabling inter dice data transmission in the context of Systems in Package (SiP) technology. The DDCM is composed of two main building blocks:

- The DDCM **controller**, responsible for managing incoming/outgoing STNoC/SBus/AMBA-AXI traffic, generating IDN segments through encapsulation and preparing them to be sent to the PHY transmitter, as well as collecting them from the PHY receiver;

- The DDCM **PHY**, responsible for transmitting output phyts across the physical link and collecting inputs phyts from the physical link.

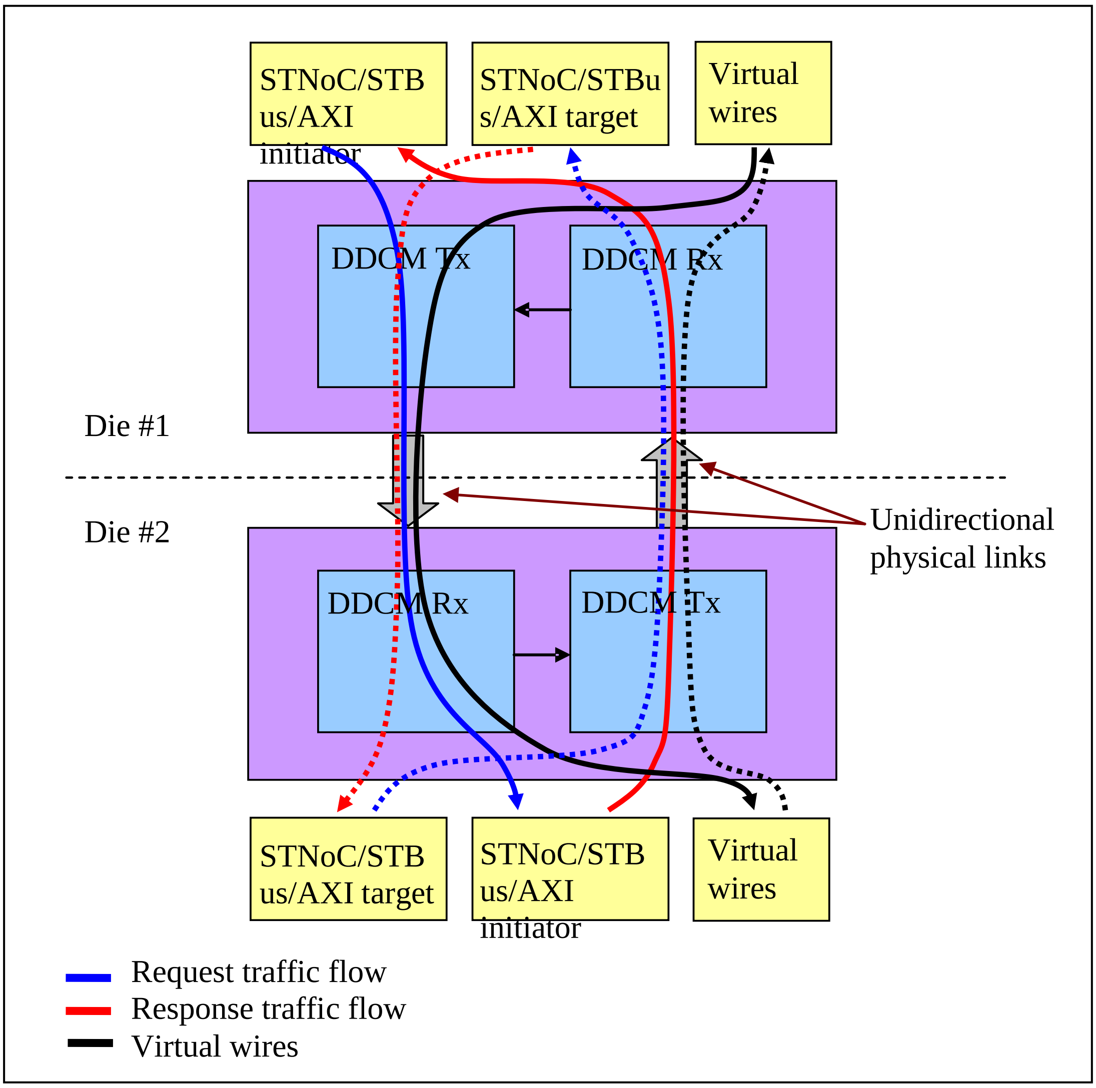

Figure 8: DDCM top level architecture and information flow

In the project, we completed the integration of the several modules into a fully working prototype that can be used for the interconnection of the chips. After synthesis and characterization flows have been carried out, the DDCM code has been synthesized for FPGA mapping, exploiting ZeBu equipment and the related environment. FPGA have been used for the traffic generation and the checking of the data emulating the STMNoC and the AXI interface. The successful integration of all the developed modules into a fully working prototype shows the feasibility of the plasmonic interconnects for future applications in which high bandwidth will be required with low power consumption.